Order Number: AN1939/D
Rev 0, 11/2001

AN1939

Clock Driver Primer — Functionality and Usage

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November, 2001

ABSTRACT

This application note focuses on the fundamentals of clock drivers, including definitions, applications, and characteristics of integrated devices. This application note is intended for the system designer that is tasked with creating a clock source for a microprocessor–based system. Although the clock may be a small portion of the system schematic, its design becomes a fundamental contributor to the overall system performance.

INTRODUCTION

Tucked away in the corner of a complex microprocessor PC board is the clock source that provides the timing for the entire PC board. This clock source may be simple or it may be complex. It may only consist of a crystal, a couple of integrated circuits, and some traces on the PC board. It may also be very complex with many clock outputs, zero–delay buffers and precise timing delays that are built into the PC board. This application note covers the basics of a clock tree design for microprocessor applications. These basics include the definitions of terms used in clock driver applications, how Phase Locked Loops (PLL) work, what makes the basic PLL into a clock driver, what distinguishes one clock driver from another, and how to select the appropriate devices for a specific application. Also, this application note covers a few of the clock tree design “gotchas.”

Applications for clock trees abound in the electronics for telecommunications and computer systems. The system requirements are for clocks of several megahertz to hundreds of megahertz. There are many common frequencies that need to be generated based upon the application for the clock. Frequencies of 33 MHz, 66 MHz, 100 MHz, and others are common in most applications. Figure 1 shows two clock trees. A simple clock tree on the left that has a crystal input of 16.66 MHz and a 200 MHz output, but is selectable from 25 MHz to 400 MHz. The clock on the right is more complex, with 16 MHz as its input, and provides as its output several clock outputs of varying drive levels. To compensate for the delay in routing the clock across a backplane or PC board, a zero–delay buffer is used to provide a clock with aligned edges.

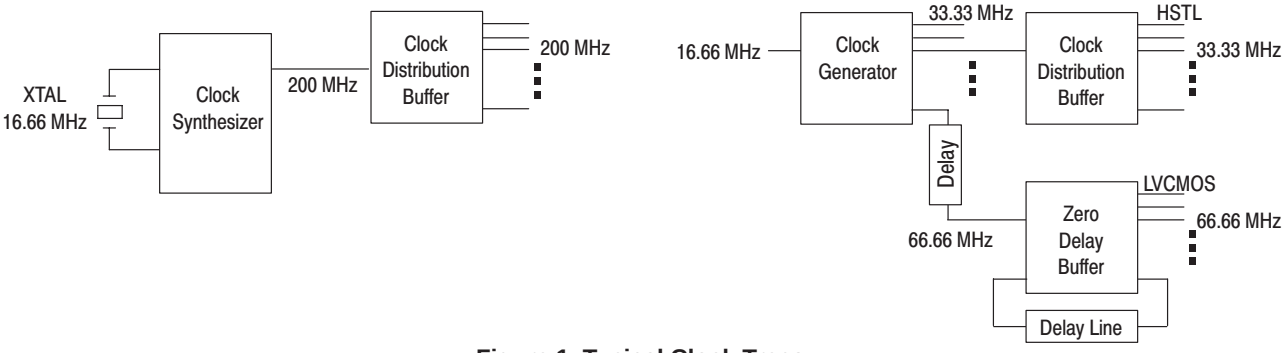


Figure 1. Typical Clock Trees

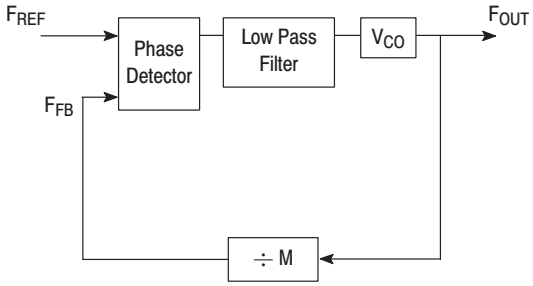
PLL CLOCK DEVICES

The Basic Phase Locked Loop

A phase locked loop or PLL is one of the fundamental elements of clock drivers. Although PLLs get used in many different electronic circuit applications, their usage in clock driver circuits dictate certain unique characteristics. It is not the intention of this application note to have complete coverage of phase lock loops. However, the fundamental operation of the PLL circuitry for clock driver applications is covered.

A phase locked loop has, as its input, a clock frequency source of which the PLL locks on to and produces, as its output, another clock signal. The output clock may be at the same frequency as the input or at some multiple of the input frequency. If the input clock should change in frequency or phase, the output clock follows this change.

A basic PLL clock architecture consists of a phase detector, a low pass filter, and a voltage–controlled oscillator or VCO, which are connected as shown in Figure 2. In addition to these blocks, the PLL has a frequency divider network which, in Figure 2, is called the M divider. This divider network is connected between the output of the VCO and one of the inputs of the phase detector. The other input to the phase detector is the reference frequency to which the PLL is to lock. The output of the PLL is F_{OUT}, which is the clock that is distributed thoughout the clock tree system.



$F_{OUT} = F_{REF} * M$

Figure 2. Basic Phase Locked Loop (PLL)

The phase detector has two inputs which are compared and used to produce a correction or error signal based upon the difference in the phase of those two inputs. One of these inputs is the previously mentioned reference frequency. The other input is the feedback signal from the VCO/divider network.

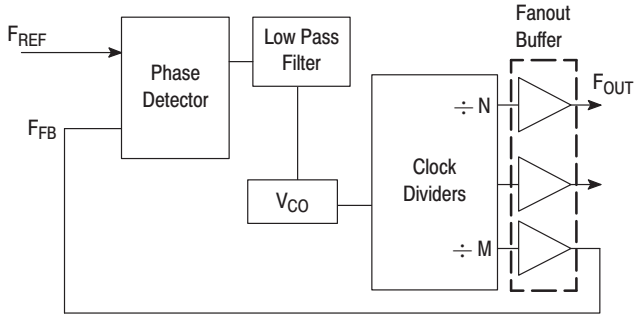
The PLL correction signal, which is the output of the phase detector, is filtered and applied to the input of a voltage–controlled oscillator or VCO. This filtered correction signal sets the VCO frequency. The output of the VCO is applied to the M (or feedback) divider and becomes the second of the two inputs to the phase detector. When the loop is in "lock," the two inputs to the phase detector are the same frequency and the same phase. This is due to the phase detector correction signal approaching zero and thus stabilizing the input control voltage to the VCO. The VCO output frequency, or F_{OUT}, becomes the reference frequency multiplied by M and continually tracks the reference frequency. The equation for F_{OUT} is the reference frequency multiplied by M. If M is 1, then the output frequency is the same as the input reference frequency.

By changing the value of M, the VCO frequency changes in increments of the reference frequency. Thus a lower reference frequency input can be multiplied up to the desired output frequency.

The VCO has a limited frequency range over which it can operate. The input frequency multiplied by the feedback divide value must produce a frequency that is within the allowable range of the VCO. If this condition is not met, the VCO is considered to be "railed" high or "railed" low and the PLL is no longer in lock.

Basic PLL Clock Driver

Figure 3 depicts additions to the previous basic PLL Clock Architecture circuitry, which creates a multi–frequency and multi–clock distribution source. The more complex divider network on the output of the VCO provides the M divide value for the feedback path to the input of the phase detector and also divides down the VCO frequency to the desired system frequency or frequencies.



$F_{OUT} = F_{REF} * M/N$

Figure 3. PLL Based Clock Generator

The outputs from this example clock generator provide multiple outputs and multiple frequencies for distribution in the application. Fanout buffers are included for each output to provide the required system drive. Also, if the device has a special feedback output, then an equivalent fanout buffer is included for the feedback path. The feedback connection may be external to the device, and this buffer equalizes the delay through the main clock outputs. By incorporating the M divider with the output dividers, the phase relationship is known between the input reference clock and the output clock(s). Also, both the feedback divider and the output divider(s) may be selectable; this allows the user to adjust the output frequency or frequencies.

Later in this application note, we will discuss how the external feedback path may also include some PC board trace delay. Design of this external trace delay allows the phase of the output clock to be aligned forward or backward (relative to the input clock phase).

A look at a Actual Clock Driver – MPC9351

Next, let's look at an actual clock driver. Figure 4 is the block diagram of a typical clock driver, the MPC9351. This device has a PLL block which contains the phase detector and VCO. The input to the MPC9351 can be either a differential clock on the PCLK and ~PCLK inputs or on the single ended input TCLK. The MPC9351 has a total of nine LVCMOS level outputs for system clock usage.

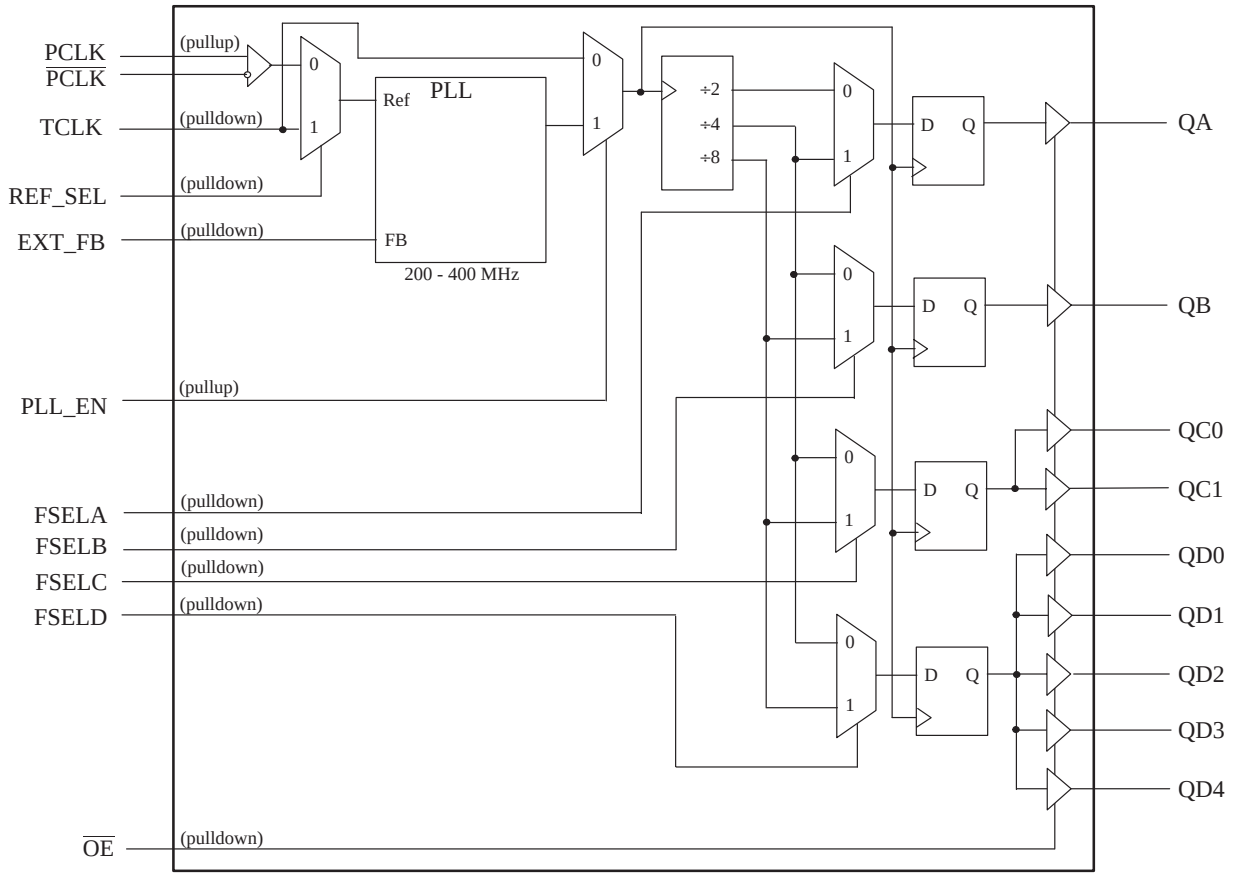
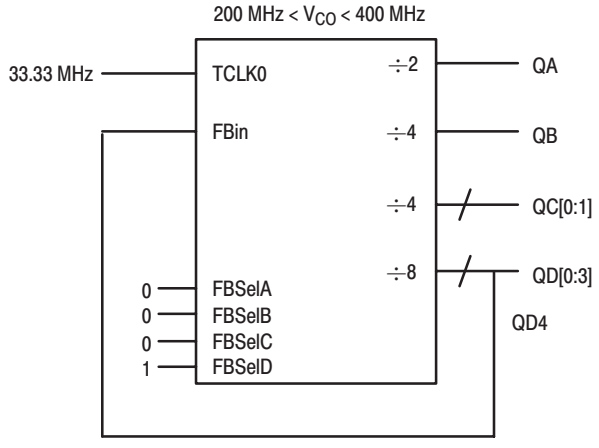


Figure 4. MPC9351 Clock Generator Block Diagram

Of special interest is the divider network and output circuitry. The VCO output of the MPC9351 is available through four banks of outputs where each bank of outputs has a selectable divide value. The first bank of outputs (labeled QA) consists of a single output. This output may provide a clock output frequency of the VCO frequency divided by either 2 or 4. The second bank of outputs (labeled QB) also consists of a single output which can be at the VCO frequency divided by 4 or 8. The third bank of 2 outputs (labeled QC0 and QC1) has the same selectable divide values of 4 or 8. Lastly, the fourth bank has four outputs (labeled QD0 – QD4) with the same divide by either 4 or 8. Although this clock driver does not have specific outputs for the feedback, typically one of the QD outputs would be used for the feedback input to the PLL. The FSELA through FSELD inputs are used to select the output divide ratios for each of the four banks.

A typical connection of the MPC9351 is shown in Figure 5. Here, a 33.33 MHz input frequency is multiplied by the feedback divide value of 8 which produces a VCO frequency of 266 MHz. This is in the allowable range of the MPC9351 VCO. The 266 MHz VCO frequency is then divided by 2 for the QA output to produce 133 MHz. Separately, the 266 MHz VCO frequency is divided by 4 for the QB output. Likewise, the 266 MHz VCO is divided by 4 for the QC outputs. This provides one clock output at 133 MHz, four clock outputs at 66.66 MHz, and four clock outputs at 33.33 MHz.



V_{CO} = 33.33 MHz * 8 = 266.66 MHz
QA = 266.66 / 2 = 133 MHz
QB = 266.66 / 4 = 66.66 MHz
QC0:1 = 266.66 / 4 = 66.66 MHz
QD0:3 = 266.66 / 8 = 33.33 MHz

Figure 5. MPC9351 Clock Generator Application

Clock Drivers–The Differences

The Motorola Advanced Clock Driver Selector Guide (SG392) has over 30 PLL clock driver devices. Each of these devices is similar in functionality but each is unique in features and the specifics of their functionality. These devices differ in the number of outputs, how the outputs are divided into banks, what feedback divider ratios are offered, and whether the device has crystal oscillator circuitry or uses an external reference input. The devices differ on whether they have differential or single–ended outputs, the frequency range of the VCO, the output duty cycle, and whether the device has an input divider for the reference. Also, the AC electrical specifications of jitter, skew, and bandwidth vary from one device to the next. The next few sections discuss some of these characteristics.

Outputs

Typically, a clock driver output is used to deliver a timing signal source to a single location in a design. If multiple locations require clock signals then multiple outputs are used. This simplifies the electrical design and the PC board design. For example, the usage of individual clock outputs eliminates the requirement of matching PC board trace lengths and worrying about trace stubs that one would have to consider when routing a single clock output to many different locations of a PC board.

Application requirements of multiple outputs result in clock drivers with different numbers of outputs. Some devices have a few outputs while others have as many as 21 individual outputs. In addition to the number of outputs, the grouping of these outputs into banks differ from one device to the next. Grouping the outputs into banks, with taps to the output divider at different values in the divider chain, allows the device to produce different output frequencies. Therefore, a device may be configured with one bank of outputs to provide a high frequency processor clock, a second bank to provide PCI clock outputs, and a third to provide specific frequencies associated with various I/O peripherals.

Input/Output Voltage Levels

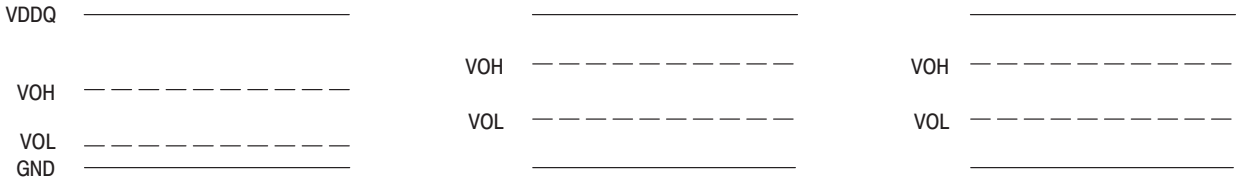
The voltage threshold levels on the input and output of the clock driver differ from one clock driver to the next. Popular logic voltage levels are LVCMOS, LVPECL and HSTL. Also, the clock drivers may have one level for the input clock and a different level for the output clock. Some clocks offer a selection of input levels. For instance, a clock input selection pin would allow the user to select between a differential pair of LVPECL inputs or a single–ended LVCMOS input.

LVCMOS is usually used as a single ended input or output. It is specified at 3.3, 2.5, and 1.8 Volts. The voltage levels are compatible to many of the inputs to microprocessors, FPGA or ASIC devices, and peripheral devices. LVCMOS is specified in JEDEC specifications EIA/JESD36 and 80.

LVPECL is typically used in differential input and output signaling. It is the low voltage, 3.3 V, version of the 5 V PECL logic specification. (PECL is the positive level specification for ECL logic.) The signal swing is approximately 600 mv and is centered at 1 volt below the supply voltage. The differential nature of LVPECL offers advantages over single ended levels. These advantages are discussed later in this application note.

The logic level specification of HSTL stands for High Speed Transceiver Logic. It is specified in EIA/JESD8–6 and is titled “A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.” It may be used as a single–ended logic interface but is more commonly used as a differential signal. HSTL has a differential voltage value Vx and common mode voltage Vcmr.

Figure 6 shows the output levels for LVCMOS, LVPECL, and HSTL. For the LVCMOS clocks, the voltage levels of 3.3, 2.5, and 1.8 are shown with the output drive levels as taken from the JEDEC specifications. Other JEDEC specifications also specify LVCMOS drive levels; however, the specifications shown here have the capability of driving 50 ohm transmission lines as would be used in clock distribution.



LVCMOS

VDDQ = 3.3	2.5	1.8	
VOH = 2.0	1.8	1.6	
VOL = 0.55	0.6	0.2	
VTT = VDDQ/2	VDDQ/2	VDDQ/2	
I = 24 ma	8 ma	100 µa	

LVPECL

VDDQ = 3.3
VOH = VDDQ – 1.025
VOL = VDDQ – 1.62
VTT = VDDQ – 2
I = ma

HSTL

VDDQ = 1.5
VOH = VDDQ – 0.5
VOL = 0.5
VTT = VDDQ/2
I = ma

Figure 6. Logic Levels

AC Characteristics – Skew and Jitter

Two important, but often misunderstood, characteristics of clock drivers are output skew and jitter. Output skew is the difference in the timing of coincident edges between outputs for multiple outputs of a clock driver. Jitter is a deviation in the frequency or period of the output clock from the specified frequency or period.

There are three different types of skew defined per the JEDEC specifications. Output–to–output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on different devices due to process variation. Finally, part–to–part skew is defined as the skew between any output on two different devices. Figure 7 illustrates output skew types for both single–ended and differential output waveforms. Typically, both output–to–output and part–to–part skew is specified on a data sheet.

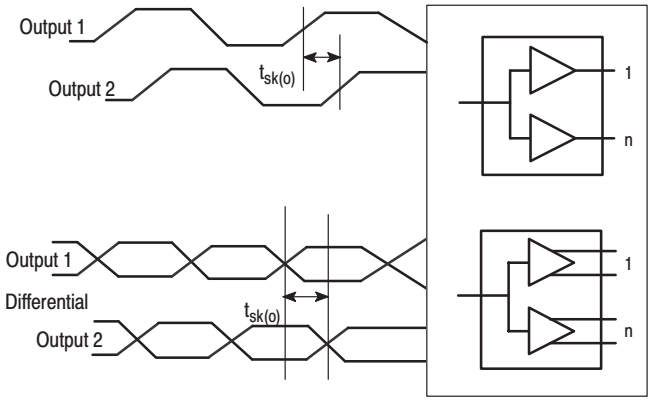


Figure 7. Output Skew

Jitter is a deviation of the edge location on the output of the clock buffer. There are three categories of jitter that are of interest: cycle–to–cycle, period, and phase jitter. One, two or all three may be specified on a clock driver data sheet. The first two are associated with both PLL and non–PLL clock drivers. The third, phase jitter, is only associated with PLL based clock drivers.

Cycle–to–cycle jitter is the difference in time between the periods of any two adjacent clock cycles. Period jitter is the deviation of time of individual periods of a signal with respect to an ideal period. Phase jitter represents the timing variation of the output with respect to the input associated with a PLL clock driver. Figure 8 shows the three types of jitter along with the associated mathematical definitions.

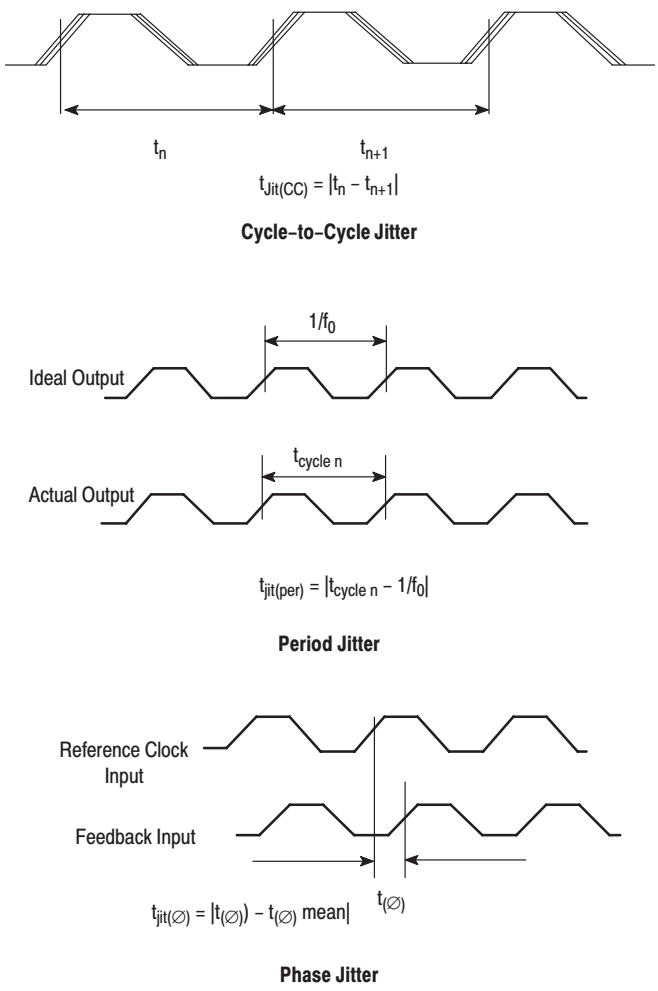


Figure 8. Clock Jitter

Additional details of skew and jitter may be found in the Motorola Application Note, AN1934.

AC Characteristics – Tracking Bandwidth

PLL clock drivers lock on to an input reference frequency and remain locked to that frequency. If that reference frequency varies, the PLL will follow that frequency and remain locked to the new input frequency. However, if the input frequency varies at a rate faster than the PLL can keep up with, then the output frequency will not track the input reference change and the PLL with appear to ignore the variation in the input frequency. The point that the PLL does not follow input frequency changes defines the upper bound of the PLL bandwidth.

The bandwidth of a PLL has a transfer characteristic much like a transfer characteristic of a lowpass filter. The bandwidth characteristic can be used to an advantage in certain clock applications. Higher frequency noise or jitter on the reference

clock input can be filtered by this characteristic. Input jitter above the bandwidth will not pass to the output of the VCO while input jitter below the bandwidth will pass through to the output.

Bandwidth of the PLL clock driver varies based upon the actual design of the PLL. One of the components that affect the bandwidth is the feedback divide ratio. Figure 9 shows a typical PLL clock generator and its bandwidth curves. PLL clock drivers that have selectable feedback divide ratios also have variable bandwidths. Higher divide ratios lower the bandwidth of the PLL clock driver.

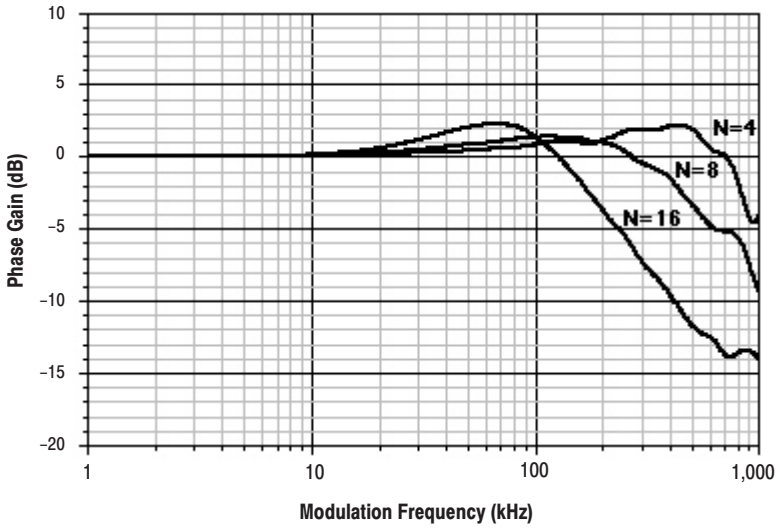


Figure 9. PLL Clock Generator Bandwidth

PLL Clock Driver Categories

Motorola PLL clock drivers are sorted into three different categories. The three categories are frequency synthesizers, clock generators, and zero–delay buffers. Although the categories are based upon the intended application, each category also reflects some uniqueness of the AC characteristics of the PLL.

Frequency Synthesizers

The first category of PLL based clock drivers is clock synthesizers. Clock synthesizers usually start with a low frequency clock source, which may come from an external source or from a crystal oscillator. This low frequency source may be further divided to produce an even lower PLL input reference frequency. With the use of the PLL, the low frequency reference frequency is multiplied up to the desired output frequency. If the device has a crystal oscillator as a reference, the oscillator circuitry would typically be part of the IC circuitry with the only required external component that of a crystal.

The clock synthesizer usually has output frequency steps with fine granularity or resolution such as 1 MHz. The overall output frequency of the clock synthesizer may be as high as 850 MHz. Examples of Motorola clock synthesizers are MPC9229, MPC9230, and MPC9239. The MPC9229 and MPC9230 each start with a midrange clock source, typically 16 MHz. This input frequency is divided by 16, which then becomes a 1 MHz input reference to the PLL. A programmable feedback divider then effectively multiplies this reference to the VCO frequency. The VCO frequency is then divided to produce the desired output frequency, as shown in Figure 10.

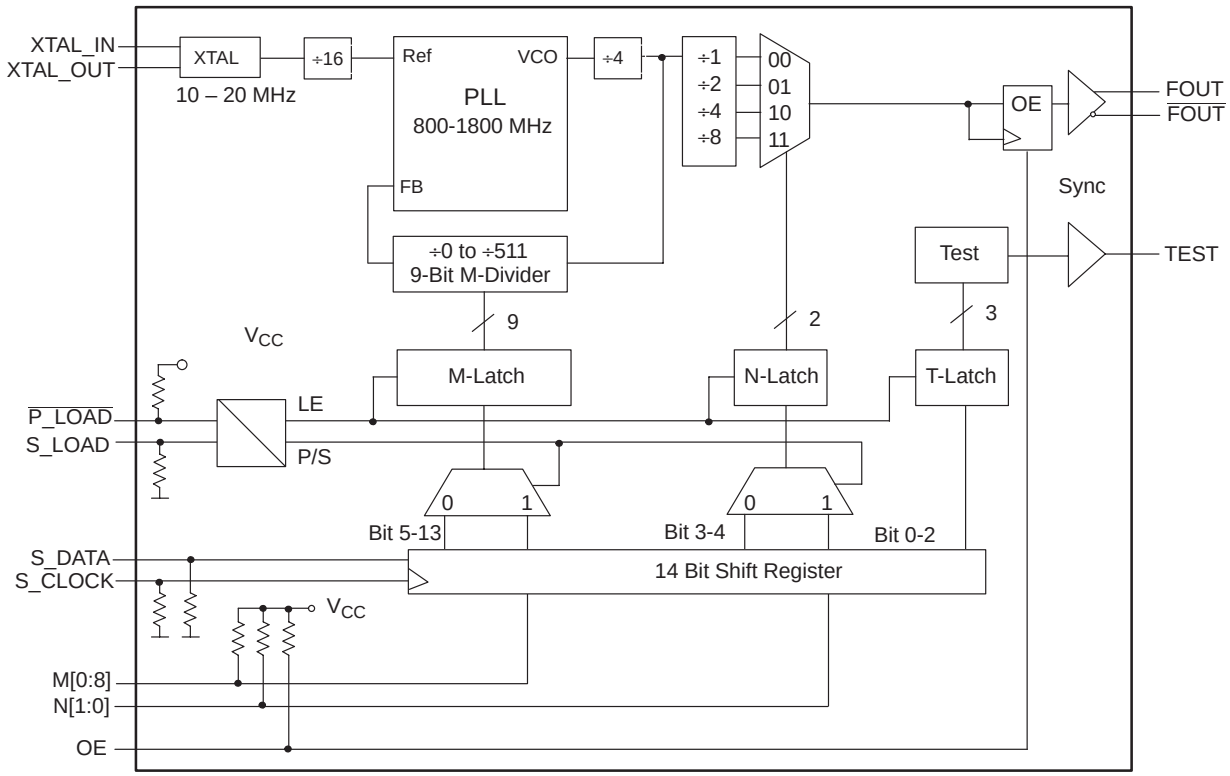


Figure 10. MPC9229 Frequency Synthesizer

A frequency synthesizer usually has a limited number of outputs; either one or two. The output frequency may be configurable in the user application. The ability to change the output frequency in small steps allows the circuit designer to do frequency margining. This is a technique where the system frequency is gradually increased/decreased while analyzing system performance.

The bandwidth of frequency synthesizers is usually the lowest of the three clock driver categories. Typical bandwidths for clock synthesizers are usually 30 to 50 kHz.

The clock synthesizer allows the system design to use a low frequency and low cost crystal oscillator and multiply the frequency up to the actual desired frequency, thus reducing the cost of the high frequency clock generation.

Clock Generators

Clock generators are used to generate clocks that are synchronous and phase aligned to an input reference clock. The category of clock generators make up the largest portion of Motorola's portfolio of the three categories of PLL based devices.

These devices typically have multiple outputs which are often grouped into multiple banks of outputs. Each bank can be set up for a different frequency. The previously discussed MPC9351 device is in the category of clock generators and, as we saw from the block diagram, it had nine outputs which were spread across four banks of outputs.

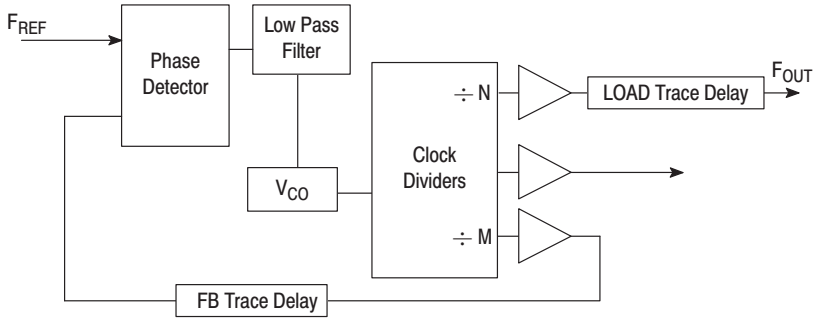
The output frequency adjustment step is usually more coarse than with the clock synthesizer. The reference frequency for a clock generator might be 15, 20, or 25 MHz, which would set the frequency step to a minimum of 15, 20, or 25 MHz. In some applications the previously discussed clock synthesizer might be used to generate the input clock for clock generators. Some clock generators have a crystal oscillator circuitry built–in.

The bandwidth of a clock generator is higher than that of a clock synthesizer and may be in the range of 300 to 500 kHz. This is considered to be a midrange bandwidth device. Clock generators maintain a phase relationship between the input clock and the output clock.

Zero–Delay Buffers

The third category of PLL clock drivers is zero–delay buffers. The concept of a zero–delay clock buffer for clock distribution may be a bit foreign, but with the use of a PLL, the concept is quite possible. The category of zero–delay buffers offers a higher bandwidth PLL than the clock generator category. Typical bandwidths are 1 to 2 MHz.

The zero–delay buffer maintains a known and precise phase relationship between the input and output clock waveforms. By adjustment of the feedback path delay, the output clock waveform may be aligned exactly to the input clock. This feedback path delay would typically be produced by the length of the PC board trace. Knowing the characteristics of the PC board material and the construction of the trace on the board can produce precise delays. Typical trace delays might be 1 to 2 ns per foot. Thus, a few inches of PC board trace can shift a clock output relative to the clock input by a significant amount. Figure 11 shows a zero–delay buffer and the equations that define the effective delay of the clock through the device. The parameter of $t(\phi)$ is the effective delay of the zero–delay buffer. The Load Trace Delay shown on one of the clock outputs is the normal trace delay that is produced by routing the clock across the PC board. The effect of this delay can be effectively eliminated with the use of a zero–delay buffer.



$$Ref\_to\_output\_delay = t_{(\varnothing)} - (t_{FB\_DELAY} - t_{LOAD\_DELAY})$$

or

$$Ref\_to\_output\_delay = t_{(\varnothing)} + (t_{LOAD\_DELAY} - t_{FB\_DELAY})$$

Figure 11. Zero–Delay Buffer

Although the zero–delay clock buffer is PLL based and shares many of the same characteristics with the clock generator, it typically has better jitter and skew performance.

Clock Distribution Buffers

In addition to the PLL based clock drivers, Motorola offers a number of devices classified as distribution buffers. There are two categories: LVCMOS single–ended output and differential clock output buffers.

Figure 12 shows two of the LVCMOS output devices. The MPC961C and the MPC961P have the same number of outputs with the same output AC characteristics; however, they differ on the type of inputs. The MPC961C has LVCMOS inputs while the MPC961P has LVPECL compatible inputs. The devices can distribute an "at frequency" clock to many locations on a PC board. Some of these clock buffers offer a built–in divider block to be able to optionally divide the input clock by two. Care should be used when using this optional divider as a half frequency output can induce additional noise and thus cause jitter to the full frequency clock.

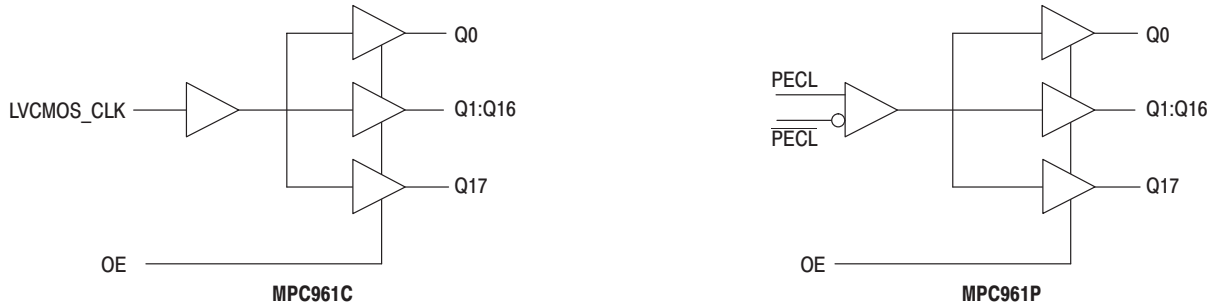


Figure 12. LVCMOS Clock Buffers, MPC942C and MPC942P

As previously mentioned, one of these categories of clock buffers have differential outputs. These outputs, and typically the input, are LVPECL or HSTL levels. Differential input and output signals offer many advantages as are discussed in the following section. An example of a differential output buffer is the MC100ES6111 differential clock driver shown in Figure 13. It has LVPECL inputs and 10 pairs of LVPECL outputs.

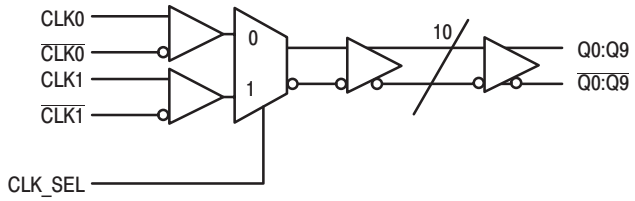


Figure 13. Differential Output Buffer MC100ES6111

Clock Redundancy

Some systems require a backup or redundant clock to be generated. Figure 14 shows two applications of a redundant clock system.

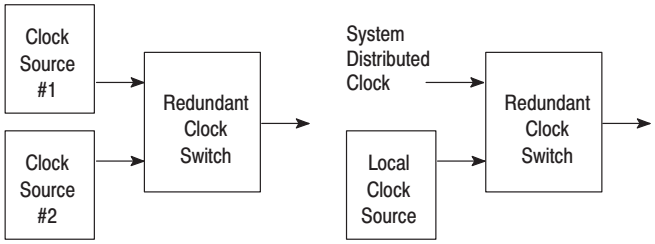


Figure 14. Redundant Clock Applications

The diagram on the left of Figure 14 shows a redundant main clock being sourced from two different central clock generation points and distributed over a cable or backplane. In this application, the redundant clock switch assures that a clock is available in the event of a removed clock board or a dead clock source.

The diagram on the right of Figure 14 shows a locally generated clock is available as a backup clock and must be switched in when the main clock fails. The redundant clock switch must make the transition from the current clock source to the backup clock in a smooth manner. While the transition takes place, the output of the clock generator must be stable with no disruption in the clock signal. The generation of runt pulses or short cycle clock periods must be avoided.

Motorola offers the MPC9993 Intelligent Dynamic Clock Switch as shown in Figure 15. The input clock sources come through the differential pair inputs of CLK0 and CLK1. The device automatically selects the good input and supplies this to the PLL. On detection of a clock failure, the device smoothly switches to the second input and continues to supply a clock to the PLL. A clock failure is defined as the input clock pins stuck high or low for at least one clock period. Status outputs from the Dynamic Switch Logic provide an indication of the current clock source.

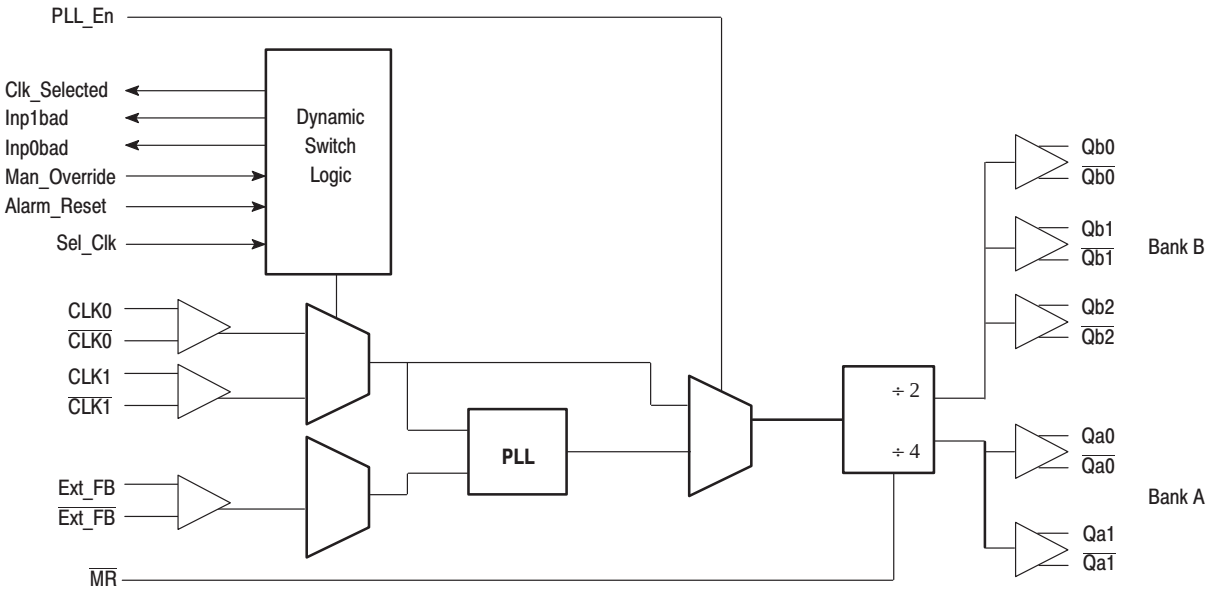


Figure 15. MPC9993 Redundant Clock Generator

The specification for the MPC9993 lists the maximum rate of period change as this clock switch is made. The data sheet also lists the typical delta period/cycle of 200ps/cycle. An actual clock switch may take as many as 100 to 200 clock cycles to complete. And as a result, the output will appear to be a "graceful" change from one clock source to the next. The automatic valid clock reference detection function may optionally be disabled and the clocks may be selected/switched manually.

The multiple outputs of the MPC9993 provide drive capability for several application system interfaces for the output clock as well as providing the feedback input to the PLL. The VCO for this device runs at 4X the input clock frequency. The outputs of the MPC9993 are grouped into two banks. Bank A is the input clock divided by 4 and has two outputs. The output of this bank is typically used for the feedback to the phase detector. Bank B consists of 3 separate outputs and is the input reference divided by 2.

Figure 16 shows a possible connection for a redundant clock system using the MPC9993. The main clock reference comes externally from the system while the backup clock comes from a MPC9229 crystal oscillator based source. One pair of the differential Bank A outputs are routed back to the EXT_FB inputs. The remaining Bank A pair of outputs and Bank B outputs are available for system usage.

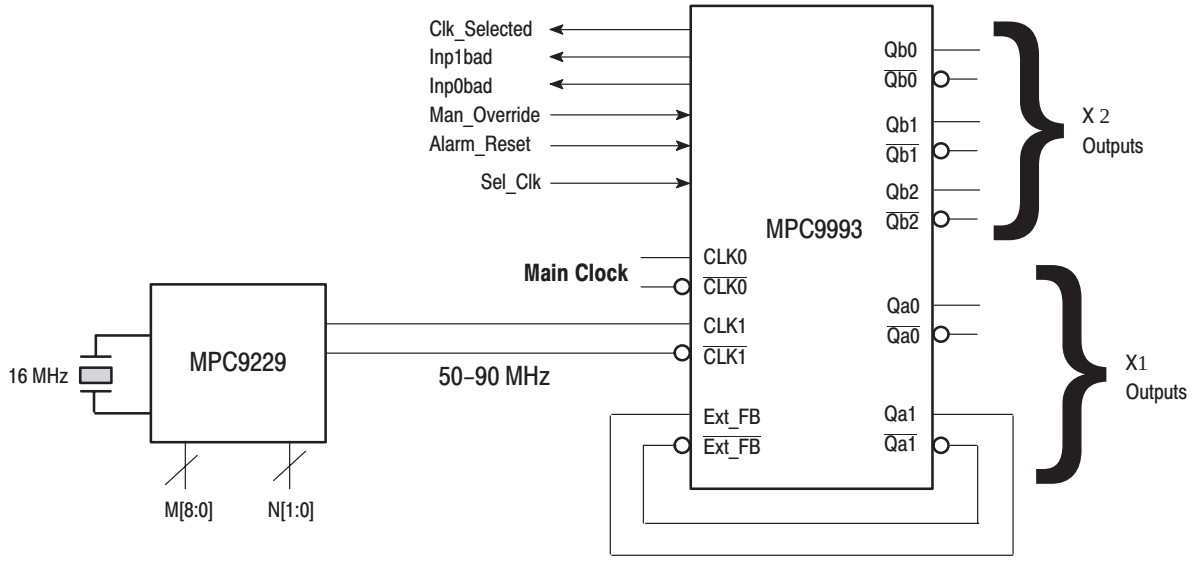


Figure 16. MPC9993 Redundant Clock Application

Figure 17 shows the “switchover” from the current clock to the backup clock. Clock A and Clock B represent the two available clock sources. When Clock A fails, this triggers the switch to Clock B. The MPC9993 slowly slews to the phase of Clock B and, after many input clock cycles, the output clock is in phase with Clock B.

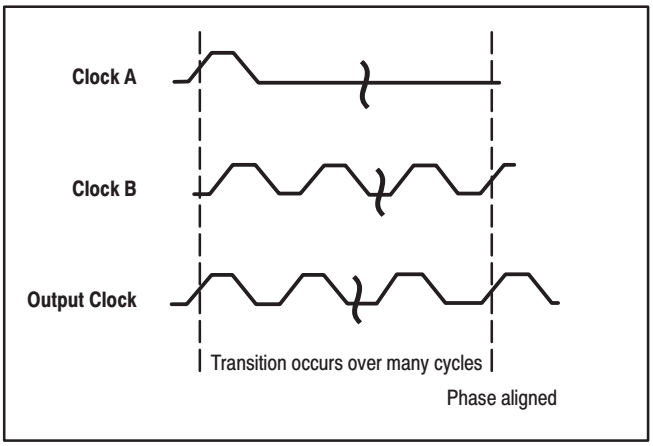


Figure 17. MPC9993 Clock Switch

Clock Tree Design and Layout

Clock performance can be predicted by understanding the clock functionality and data sheet parameters for jitter and skew, but the overall clock performance is highly dependent on design of the clock circuitry and its environment on the PC board. The following sections point out areas of clock design that need special attention to ensure the best clock performance obtainable from the design. The first of these topics is that of power supplies.

Power Supplies

Noisy power supplies have an affect on clock trees by generating jitter on the clock outputs. This is due to the noise on the power supply affecting the input–switching threshold and/or modulating the input control voltage to the VCO. Many of the Motorola clock generators offer separate PLL power pins, allowing for the isolation of the PLL power from the output driver supply. Use lots of high quality filter caps and (physically) place them as close to the clock driver package as possible.

Most of the PLL clock driver devices are analog devices. These drivers are designed with separate power supply connections for the outputs and the PLL analog circuitry. The example shown in Figure 18 separates out the analog supply, VCCA, from the supply driving the rest of the chip. A simple RC filter decreases the noise injected into the analog supply pin, minimizing the jitter due to power supply noise. The value of R_S must be calculated based up the maximum ICCA current. Filter caps should be of high quality for best overall frequency characteristics. Noisy power supplies may significantly compromise good clock tree designs on paper.

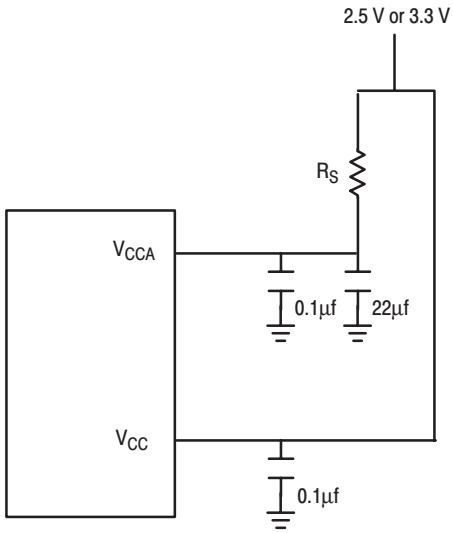


Figure 18. Power Supply Filtering

PC Board Trace Impedance Matching

In system applications utilizing high frequency clocks and/or microprocessor bus speeds, the PC board traces are characteristic transmission lines and must be treated appropriately. Termination of the transmission line must be done in order to minimize reflections and maintain proper signals in the system. Either parallel termination or series termination may terminate clock–signaling lines. Each method has advantages.

Parallel termination places a resistor on the load end of the transmission line. The value of the termination resistor is equal to the impedance of the transmission line. Figure 19 depicts the parallel termination on a clock line with the associated waveform of a clock edge propagating down the line. Since the parallel termination is equal to the characteristic impedance of the line, there is no reflection when the clock edge reaches the load.

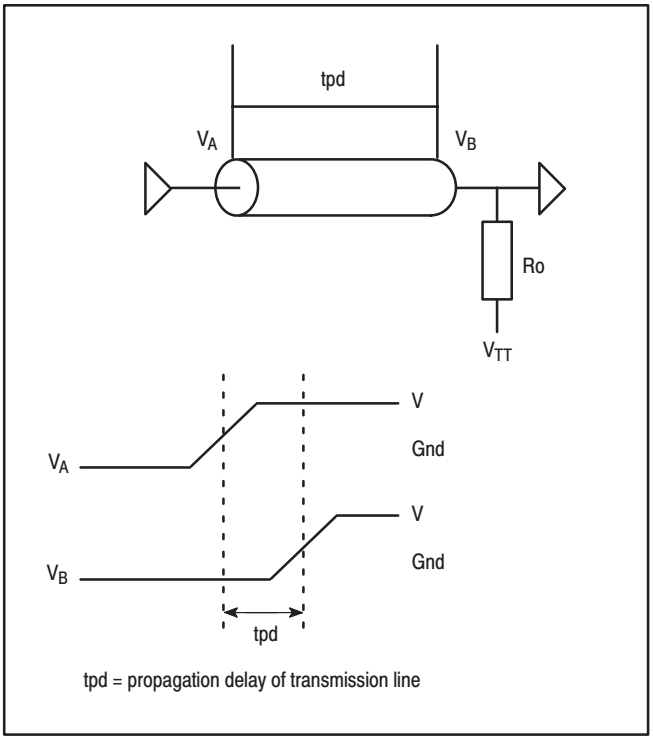


Figure 19. Parallel Termination with Waveform

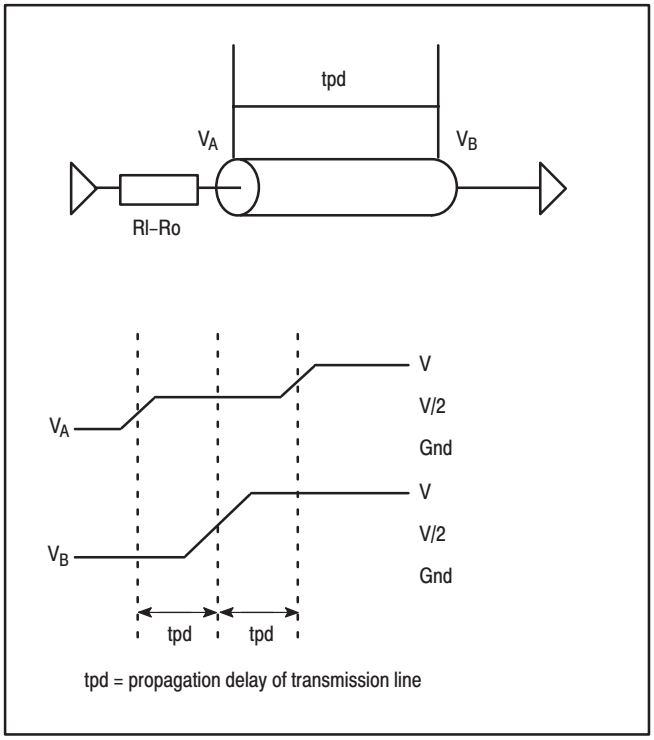


Figure 20. Series Termination with Waveform

Series termination places a resistor on the source end of the transmission line and in series with the transmission line. The resistor value is chosen such that the output impedance of the clock driver output buffer, plus this resistor, equals the characteristic impedance of the transmission line. No termination impedance is placed at the load end of the transmission line.

Figure 20 shows the waveform of a clock edge as it appears on the output of the clock driver and as it propagates down the transmission line. As the clock edge starts down the transmission line, the series resistor and the impedance of the transmission line act as a voltage divider causing an edge of amplitude V/2 to be propagated. After tpd time period, the edge arrives at the load end of the transmission line. This point appears to be an open line to the propagated edge causing a reflection of the edge of amplitude V/2 to be sent back to the source. On arrival at the source, the reflected waveform encounters the series termination which damps the reflected voltage and the waveform establishes a steady state. Since the voltage at the source is V and the voltage at the load is also V, there is no current flow down the transmission line other than the initial charging of the line.

The advantage of series termination is that there is no steady state loading on the line and thus the steady state drive requirements of the clock driver is low.

Single–Ended Verses Differential Clock lines

Distribution of clock signals via differential paths has several advantages over single–ended clocks. Most of these advantages relate to noise immunity.

Even though the differential clock complicates the routing of the PC board by doubling the number of traces, differential clocks may ease the PC board layout due to ground plane issues.

All currents are in the signal traces for the differential pair and not in the underlying ground plane. Thus, the effects of breaks or discontinuities in the PC board ground plane within the vicinity of the clock drive circuitry are minimized. In addition, since one output or the other is always driving a signal, the constant supply current leads to Vcc/Ground Bounce reduction.

There are many detailed references dealing with the subject of PC board layout and transmission line characteristics, which should be consulted for additional information.

Steps in Selecting a Clock Driver

Now that we have looked at the definitions, characteristics, and categories of clock driver devices, the question is, “How do I choose the devices or devices that fit into my application?” The following list of questions should be answered in order to understand what type of clock drivers are required.

1. What are the input and output requirements for logic levels in the application?
2. Does the application have or require differential input or output?
3. What is the clock source? Is it externally provided? What is the frequency?
4. Is a PLL based clock driver required?
5. What are the output frequency requirement(s)?
6. What number of outputs at each frequency is required?

Once these user application questions are answered, the next step in the clock design is to consult the Advanced Clock Driver Selector Guide for devices that match these requirements. If a PLL clock driver is needed, determine the feedback divide ratio and determine if the allowable VCO range is met. Once the VCO frequency is determined, next determine the output divide ratios required meeting output frequency requirement(s). Once a potential device has been selected, evaluate the jitter and skew specifications of that device based upon the system parametrics.

SUMMARY

Whether the clock design is simple or complex, the performance of the clock circuitry can best be optimized by an understanding of the parameters of the clock devices involved in the design. Many parameters may be of little or no importance to the design; however, the designer should understand these parameters and make that determination. Finally, clock tree design should be given proper attention to ensure the reliability of the system design.

CLOCK DRIVER RESOURCES

AN1934/D – Effects of Skew and Jitter on Clock Tree Design
DL207/D – Advanced Clock Drivers Device Data Book
SG392/D – Advanced Clock Drivers Selector Guide

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